

Claims

We claim:

1. A clock synchronization circuit for generating an output clock signal that is substantially in synchronization with a reference clock signal when in an in-synchronization state with a phase difference between the two clock signals of less than a predetermined value, the clock synchronization circuit comprising:
 - a programmable delay element coupled to the reference clock signal for introducing an adjustable delay in the reference clock signal to produce a delay-adjusted delayed output clock signal that becomes increasingly closer to being in synchronization with the reference clock signal; and
 - a phase detector coupled to the reference clock signal and the delay-adjusted delayed output clock signal for detecting the phase difference between the two clock signals and for generating an in-synchronization signal when the in-synchronization state is reached.
2. A clock synchronization circuit according to Claim 1; wherein the in-synchronization signal is a pulse having a pulse width sufficient to interrupt a microprocessor.
3. A clock synchronization circuit according to Claim 1; wherein the phase detector comprises:
 - a pulse generator that produces a pulse of variable width when the output clock signal approaches the in-synchronization state as the adjustable delay is increased; and
 - a latch that is triggered by the pulse to generate the in-synchronization signal when the width of the pulse reaches a pulse width Z required to trigger the latch.

1 4. A clock synchronization circuit according to Claim 3; wherein the latch
2 is a D-type latch.

3
4 5. A clock synchronization circuit according to Claim 3; wherein the pulse
5 generator comprises:

6 means for producing a window of a known width Y that is at
7 least equal to the pulse width Z; and

8 means for generating a signal (IN1) from the delay-adjusted
9 delayed output clock signal whose mark of a cycle is brought to overlap
10 with the window when the adjustable delay is increased to produce the
11 pulse.

12
13 6. A clock synchronization circuit according to Claim 5; wherein the
14 means for producing the window is a three-input AND gate having a first input
15 coupled to the reference clock signal, a second input coupled to an inverted
16 reference clock signal that is delayed by Y and the third input is coupled to the
17 reference clock signal delayed substantially by 2Y.

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19 7. A clock synchronization circuit according to Claim 6; wherein the in-
20 synchronization state is reached when the pulse width reaches a width Y-X
21 that is equal to the pulse width Z; whereby the in-synchronization signal is
22 generated.

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24 8. A clock synchronization circuit according to Claim 6; wherein the
25 second input of the three-input AND gate is coupled to an inverted reference
26 clock signal that is delayed by Y+D whereby D is a delay provided by a delay
27 element.

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29 9. A clock synchronization circuit according to Claim 8; wherein the
30 bounds of the phase difference X is given by a worst case phase lead of
31 $Y_{\max} - Z_{\min}$ and a worst case phase lag of $Y_{\min} - Z_{\max}$ depending on the
32 values of Y and Z, wherein

1 Ymax and Ymin are the maximum and minimum delays of a
2 NOT gate respectively; and

3 Zmax and Zmin are the maximum and minimum pulse widths
4 required to trigger the latch respectively.
5

6 10. A clock synchronization circuit according to Claim 1; wherein the clock
7 synchronization circuit is implemented in a programmable gate array.
8

9 11. A clock synchronization circuit according to Claim 8; wherein the delay-
10 adjusted output clock signal is carried on a trace on a printed circuit board on
11 which the programmable gate array is mounted.
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13 12. A method of generating a delayed output clock signal that is
14 substantially in synchronization with a reference clock signal when the
15 delayed output clock signal has a predetermined phase difference X with the
16 reference clock signal, the method comprising:

17 inverting and delaying by a first delay the reference clock signal
18 to produce an intermediate clock signal, wherein this intermediate clock
19 signal cooperates with the reference clock signal to provide a window
20 of width equal to the predetermined delay;

21 introducing an adjustable delay in the intermediate clock signal
22 to produce a delay-adjusted delayed output clock signal;

23 inverting and delaying by a second predetermined delay Y the
24 delay-adjusted delayed output clock signal to produce a reference
25 clock signal delayed by the first delay and the second predetermined
26 delay Y;

27 increasing the adjustable delay to bring a cycle of the delay-
28 adjusted delayed output clock signal to be increasingly in
29 synchronization with a subsequent cycle of the reference clock signal
30 until a synchronization condition is reached where a mark of a cycle of
31 the reference clock signal delayed by the first delay and the second
32 predetermined delay Y appears in the window to indicate that the

1 delay-adjusted delayed output clock signal leads the reference clock
2 signal by the phase difference X that is equal to the second
3 predetermined delay Y.
4

5 13. A method according to Claim 12; wherein increasing the adjustable
6 delay comprises increasing the adjustable delay by a known delay step D
7 each time the adjustable delay is incremented.
8

9 14. A method according to Claim 13; further comprising increasing the
10 delay by a further number of delay steps corresponding to Y/D to bring the
11 delayed-adjusted delayed output clock signal to be more in synchronization
12 with the reference clock signal after the synchronization condition is reached.
13

14 15. A method according to Claim 12; wherein increasing the adjustable
15 delay comprises increasing the adjustable delay until a portion of the mark
16 corresponding to a width of Z appears in the window; whereby the delay-
17 adjusted delayed output clock signal leads the reference clock signal by a
18 phase difference X that is equal to the second predetermined delay Y minus
19 the width Z.
20

21 16. A method according to Claim 13; wherein Y is smaller than Z and the
22 first delay is greater than Z and wherein increasing the adjustable delay
23 comprises increasing the adjustable delay until a portion of the mark
24 corresponding to a width of Z appears in the window; whereby the delay-
25 adjusted delayed output clock signal lags the reference clock signal by a
26 phase difference X that is equal to the width Z minus the second
27 predetermined delay Y.